

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:
a die pad;
5 a die mounted on the die pad;
a plurality of outer leads electrically connected to
electrodes of the die by bonding wires, respectively; and
a sealing member sealing therein the die, the
bonding wires, parts of the outer leads and a part of the
10 die pad, and having an upper surface on the side of the
die and a lower surface on the side of the die pad;
wherein the outer leads have upper electrical
connecting surfaces on the side of the upper surface of
the sealing member, and lower electrical connecting
15 surfaces on the side of the lower surface of the sealing
member, respectively, and the outer leads have a height
from a plane including the lower surface of the sealing
member greater than that of the upper surface of the
sealing member from the same plane.

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2. The semiconductor package according to claim 1,
wherein the upper electrical connecting surfaces of the
outer leads formed on the side of the upper surface of the
sealing member lie outside a projection region of the
25 upper surface of the sealing member.

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3. The semiconductor package according to claim 1,
wherein the sealing member has four sides, and the outer
leads are formed on the four sides of the sealing member.

4. The semiconductor package according to claims 1,
wherein the outer leads are formed in an L-shape.

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5. A semiconductor device comprising:
a printed wiring board; and
a plurality of semiconductor packages, stacked up on
5 the printed wiring board with outer leads included
therein; wherein each of the plurality of semiconductor
packages comprises,
a die pad;
a die mounted on the die pad;
10 the outer leads electrically connected to electrodes
of the die by bonding wires, respectively; and
a sealing member sealing therein the die, the
bonding wires, parts of the outer leads and a part of the
die pad, and having an upper surface on the side of the
15 die and a lower surface on the side of the die pad;
wherein the outer leads have upper electrical
connecting surfaces on the side of the upper surface of
the sealing member, and lower electrical connecting
surfaces on the side of the lower surface of the sealing
20 member, respectively, and the outer leads have a height
from a plane including the lower surface of the sealing
member greater than that of the upper surface of the
sealing member from the same plane.

25 6. The semiconductor device according to claim 5,
wherein the upper electrical connecting surfaces of the
outer leads formed on the side of the upper surface of the
sealing member lie outside a projection region of the
upper surface of the sealing member.

30 7. The semiconductor device according to claim 5,
wherein the sealing member has four sides, and the outer

leads are formed on the four sides of the sealing member.

8. The semiconductor device according to claims 5,
wherein the outer leads are formed in an L-shape.

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9. A semiconductor device comprising:
a printed wiring board; and
a semiconductor package, mounted on the printed
wiring board with a upper surface of a sealing member
10 thereof facing the printed wiring board and outer leads
thereof connected to electrodes formed on the printed
wiring board; wherein each of the plurality of
semiconductor packages comprises,
a die pad;
15 a die mounted on the die pad;
the outer leads electrically connected to electrodes
of the die by bonding wires, respectively; and
the sealing member sealing therein the die, the
bonding wires, parts of the outer leads and a part of the
20 die pad, and having the upper surface on the side of the
die and a lower surface on the side of the die pad;
wherein the outer leads have upper electrical
connecting surfaces on the side of the upper surface of
the sealing member, and lower electrical connecting
25 surfaces on the side of the lower surface of the sealing
member, respectively, and the outer leads have a height
from a plane including the lower surface of the sealing
member greater than that of the upper surface of the
sealing member from the same plane.

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10. The semiconductor device according to claim 9,
wherein the upper electrical connecting surfaces of the

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outer leads formed on the side of the upper surface of the sealing member lie outside a projection region of the upper surface of the sealing member.

5 11. The semiconductor device according to claim 9, wherein the sealing member has four sides, and the outer leads are formed on the four sides of the sealing member.

10 12. The semiconductor device according to claims 9, wherein the outer leads are formed in an L-shape.

13. The semiconductor device according to claim 9, wherein the die pad of the semiconductor package is provided on its exposed surface with a cooling fin.

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